REMARKS

Claims 1-28 are pending in the instant application. Claims 1, 3, 4, 5, 7, 11, 13, 14, 15, 16, 17, 18, 20, 22, 23, 24, 25, 26, 27 are amended. Claims 2, 12 and 21 are cancelled. Claims 1-28 are rejected. No new matter has been added.

103 Rejections

Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are set forth in Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are neither anticipated nor rendered obvious by Dye in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a controller chip. Claim 1 is presented below in it's entirety for the Examiner's convenient reference.

> 1. A controller chip comprising:
>
> a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and
>
> first in first out (FIFO) buffer coupled to the graphics engine, the FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the integral interface, and manages the FIFO buffer via the integral interface.

Independent Claims 11 and 20 contain limitations similar to those contained in Claim 1. Claims 2 (cancelled), 3, 6, 9 and 10 depend from Claim 1, Claims 12 (cancelled), 13, 16 and 17 depend

from Claim 11, and Claims 21(cancelled), 25 and 26 depend from Claim 20 and set forth additional limitations of the claimed invention.

Dye in view of Davis et al. does not anticipate or render obvious the embodiments of the present invention as set forth in Claims 1, 11 and 20. Applicant respectfully submits that Dye does not teach or suggest each of the limitations of Claims 1, 11 and 20 and Davis does not remedy the deficiencies of Dye. In particular, Dye does not anticipate or render obvious a controller chip that includes a graphics engine a memory, and a first in first out (FIFO) buffer wherein the graphics engine is operative to manage the memory and wherein "the graphics engine comprises an integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not anticipate or render obvious a controller chip that includes a graphics engine that "receives commands from the CPU via the integral interface, and manages the first in first out (FIFO) buffer via the integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). And, Davis does not remedy the aforementioned deficiencies of Dye.

It should be appreciated that in order to anticipate or render obvious the embodiment of the invention that is set forth in Claim 1 (Claims 11 and 20 contain similar limitations) the cited references must teach or suggest, either expressly or inherently, in addition to all of the other limitation of Claim 1 (Claims 11 and 20 contain similar limitations), a graphics engine that: (1) includes an integral interface; (2) receives commands from a CPU via the integral interface that is a part of the engine; and (3) manages a first in first out (FIFO) buffer via the same integral interface. The Applicant respectfully submits that such a system structure and operation is neither shown nor suggested by Dye.

Dye discloses a memory controller that includes embedded data compression and decompression engines and that uses data compression to reduce system bottlenecks. However,

the system structure that is disclosed by Dye is distinct from that of the system which is set forth in the Applicant's claims and cannot support significant aspects of the functionality of the system that is defined in Applicant's claims. Specifically, Dye does not show a controller graphics engine that includes an integral interface that is actually physically integrated into the graphics engine through which commands from a CPU are received and via which a first in first out (FIFO) buffer is managed as is set forth in Claim 1 (independent Claims 11 and 20 contain similar limitations).

It should be noted that those components of the Dye system that are intended to represent engines are clearly delineated as such (e.g., labeled as execution engine 210 and graphics engine 212 in Figure 5 of Dye). Neither the execution engine 210 nor the graphics engine 212 are described in the text or shown in the drawings of the Dye reference to have an interface integrally contained therein via which a FIFO buffer is managed. This should be contrasted with Applicant's specification that describes as is shown in Applicant's Figure 4 that the recited interface through which FIFO buffer 306 is managed is actually a physically integrated part of the recited graphics engine of Claim 1 (independent Claim 11 contains similar limitations).

In the Office Action, the integrated memory controller (IMF) 140 is equated with the recited graphics engine, and I/F logic 202 is equated with the recited interface via which a FIFO buffer is managed. Moreover, the element equated in the Office Action with the FIFO buffer is instruction storage decode logic 230. Applicant respectfully submits that a FIFO buffer is a well known type of storage component and would not be confused with instruction storage decode logic 230 by one of ordinary skill in the art. Accordingly, there is no structure disclosed by Dye that can be reasonably equated to the recited FIFO buffer that is controlled via an interface that is integral with a graphics engine. Therefore, even if the strained characterization of the IMF as a graphics engine is accepted as contended in the office Action, all the limitations of the Claims would still not be met because controlling a FIFO buffer via an interface is not disclosed by Dye.

Davis et al. does not teach or suggest a modification of Dye that remedies the deficiencies of Dye outlined above. More specifically, Davis et al. does not teach or suggest a controller chip that includes a graphics engine, a memory, and a first in first out (FIFO) buffer wherein the graphics engine is operative to manage the memory and wherein "the graphics engine comprises an integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not teach or suggest a controller chip that includes a graphics engine that "receives commands from the CPU via the integral interface, and manages the first in first out (FIFO) buffer via the integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations).

Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division channels of a digital carrier signal. It should be appreciated that the Davis et al. reference is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. As a result, nowhere in the Davis et al. reference is there shown a controller chip engine that receives commands via an integral interface and manages a first in first out (FIFO) buffer via the interface where the interface is actually a part of the graphics engine itself as is set forth in Claims 1, 11 and 20. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye and Davis et al. either alone or in combination.

Therefore, Applicant respectfully submits that Claims 1, 11 and 20 are in condition for allowance. Accordingly, Applicant respectfully submits that Dye and Davis et al. either alone or in combination, do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 3, 6, 9 and 10 dependent on Claim 1, Claims 13, 16 and 17 dependent on Claim 11, and Claims 25 and 26 dependent on Claim 20. Claims 2, 3, 6, 9, 10, 12,

13, 16, 17, 21, 25 and 26 are allowable as they are dependent on allowable base claims. As mentioned above Claims 2, 12 and 21 are cancelled herein.

Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169) and further in view of an Official Notice. The Applicant has reviewed the cited references and respectfully submits that embodiments of the present invention as are set forth in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al. and further in view of the Official Notice. It should be appreciated that the Official Notice is concerned with the obviousness of utilizing various FIFO buffer geometries but does not address the deficiencies of either Dye or Davis et al. as outlined above. Consequently, the embodiments of the Applicant's invention as set forth in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye in view of Davis et al. and further in view of the Official Notice as these Claims are dependent on base Claims 1, 11 and 20 whose patentability are discussed above.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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